wherein an [the] output of said second circuit is coupled to an [the] output of said first circuit.

9. (amended) The semiconductor integrated circuit according to claim 7, wherein said second circuit includes a [second] MOS transistor whose source-drain path is coupled between the external supply voltage and the output of said first circuit.

11. (amended) The semiconductor integrated circuit according to claim 7, wherein said second circuit forms a current path between the external voltage and the output of said first circuit [supplies the output voltage thereof] during the aging test.

12. (amended) The semiconductor integrated circuit according to claim 8, wherein said second circuit forms a current path between the external voltage and the output of said first circuit [supplies the output voltage thereof] during the aging test.

13. (amended) The semiconductor integrated circuit according to claim 9, wherein said second circuit forms a current path between the external voltage and the output of said first circuit [supplies the output voltage thereof] during the aging test.

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14. (amended) The semiconductor integrated circuit according to claim 10, wherein said second MOS transistor is turned on [circuit supplies the output voltage thereof] during the aging test.

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15. (amended) A semiconductor integrated circuit comprising:

a first circuit[,] supplied with an external supply voltage, said first circuit [which] outputs a voltage changing at a first rate which is smaller than the changing rate of the external supply voltage, when the external supply voltage changes [in] to a voltage [level] larger than a predetermined voltage;

an internal circuit supplied with an output voltage of said first circuit;

a second circuit, for use in performing an aging test of said internal circuit, and being supplied with the external supply voltage, [which] said second circuit outputs a voltage changing at a second rate which is larger than the first rate ;[and

an internal circuit supplied with the output voltage of said first circuit;]

wherein an [the] output of said second circuit is coupled to an [the] output of said first circuit.

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17. (amended) The semiconductor integrated circuit according to claim 15, wherein said second circuit includes

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a [second] MOS transistor whose source-drain path is coupled between the external supply voltage and the output of said first circuit.

19. (amended) The semiconductor integrated circuit according to claim 15, wherein said second circuit forms a current path between the external voltage and the output of said first circuit [supplies the output voltage thereof] during the aging test.

20. (amended) The semiconductor integrated circuit according to claim 16, wherein said second circuit forms a current path between the external voltage and the output of said first circuit [supplies the output voltage thereof] during the aging test.

21. (amended) The semiconductor integrated circuit according to claim 17, wherein said second MOS transistor is turned on [circuit supplies the output voltage thereof] during the aging test.

22. (amended) The semiconductor integrated circuit according to claim 18, wherein said second MOS transistor is turned on [circuit supplies the output voltage thereof] during the aging test.

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23. (amended) A semiconductor integrated circuit comprising:

a first circuit[,] supplied with an external supply voltage, said first circuit [which] outputs a voltage changing at a first rate which is smaller than the changing rate of the external supply voltage, when the external supply voltage changes to [in] a voltage [level] larger than a predetermined voltage;

an internal circuit supplied with an [the] output voltage of said first circuit as an operation voltage; and

a second circuit for supplying a voltage larger than the operation voltage to said internal circuit during an aging test and having a MOS transistor whose source-drain path is coupled between the external supply voltage and an output of said first circuit;

wherein the MOS transistor is turned on when said internal circuit requires [needs] a larger voltage than the voltage changing at the first rate during the aging test.

24. (amended) The semiconductor integrated circuit according to claim 23, wherein said first circuit includes a first MOS transistor whose drain is coupled to an [the] output of said first circuit, and

wherein said first circuit has a feedback circuit between the gate of said [first] MOS transistor and the output of said first circuit.

25. (amended) The semiconductor integrated circuit according to claim 23, wherein the MOS transistor of said second circuit is turned on during the aging test.

26. (amended) The semiconductor integrated circuit according to claim 24, wherein the MOS transistor of said second circuit is turned on during the aging test.

27. (amended) A semiconductor integrated circuit comprising:

a first circuit[,] supplied with an external supply voltage, said first circuit [which] outputs a voltage changing at a first rate which is smaller than the changing rate of the external supply voltage, when the external supply voltage changes to [in] a voltage [level] larger than a predetermined voltage;

an internal circuit supplied with an [the] output voltage of said first circuit; and

a second circuit having a MOS transistor whose source-drain path is coupled between the external supply voltage and an [the] output of said first circuit;

wherein the MOS transistor is turned on to provide a larger voltage than the voltage changing at the first rate.

28. (amended) The semiconductor integrated circuit according to claim 27, wherein said first circuit includes a

first MOS transistor whose drain is coupled to an [the] output of said first circuit, and

wherein said first circuit has a feedback circuit between the gate of said first MOS transistor and the output of said first circuit.

29. (amended) The semiconductor integrated circuit according to claim 27, wherein the MOS transistor of said second circuit is turned on during an aging test.

30. (amended) The semiconductor integrated circuit according to claim 28, wherein the MOS transistor of said second circuit is turned on during an aging test.

31. (amended) The semiconductor integrated circuit according to claim 7, wherein an [the] amplitude of a [an] [output] voltage at the output of said first circuit [is to] enables the aging test to be performed by [enlarging] increasing the amplitude of the external supply voltage relative to an amplitude of normal operation voltage.

33. (amended) The semiconductor integrated circuit according to claim 7, further comprising:

a third [fourth] circuit [operated by] supplied with the external supply voltage, said third circuit [which] transfers a signal to said internal circuit.

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35. (amended) The semiconductor integrated circuit according to claim 33, wherein said third [fourth] circuit has a larger device than a device [that] of said internal circuit.

36. (amended) The semiconductor integrated circuit according to claim 35, wherein said larger device of said third [fourth] circuit is a MOS transistor which has a larger thickness of the gate insulator than that of a MOS transistor of said internal circuit.

37. (amended) The semiconductor integrated circuit according to claim 35, wherein said larger device of said third [fourth] circuit is a MOS transistor which has a longer gate length than that of a MOS transistor of said internal circuit.

38. (amended) The semiconductor integrated circuit according to claim 7, wherein said predetermined voltage is determined by a reference voltage [reference].

39. (amended) The semiconductor integrated circuit according to claim 38, wherein said [voltage] reference voltage is determined by using a threshold voltage of a first MOS transistor.

40. (amended) The semiconductor integrated circuit according to claim 17, wherein a [load] capacitance of a load of said [internal circuit] first circuit changes in accordance with a signal, said load includes said internal circuit.

41. (amended) The semiconductor integrated circuit according to claim 15, wherein an [the] amplitude of [the output] a voltage at the output of said first circuit enables the aging test to be performed by increasing [enlarging] the amplitude of the external supply voltage relative to an amplitude of normal operation voltage.

42. (amended) The semiconductor integrated circuit according to claim 15, wherein said second circuit causes a [makes the] changing rate of a voltage at the output [voltage] of said first circuit to be larger than the first rate during the aging test.

43. (amended) The semiconductor integrated circuit according to claim 15, further comprising:

a third circuit[,] supplied with the external supply voltage, [which] said third circuit transfers a signal to said internal circuit.

45. (amended) The semiconductor integrated circuit according to claim 43, wherein said third circuit has a larger device than a device [that] of said internal circuit.

48. (amended) The semiconductor integrated circuit according to claim 15, wherein said predetermined voltage is determined by a reference voltage [reference].

49. (amended) The semiconductor integrated circuit according to claim 48, wherein said reference voltage [reference] is determined by using threshold voltage of a MOS transistor.

50. (amended) The semiconductor integrated circuit according to claim 15, wherein a [load] capacitance of a load of said [internal circuit] first circuit changes in accordance with a signal, said load includes said internal circuit.

51. (amended) The semiconductor integrated circuit according to claim 23, wherein an [the] amplitude of [the output] a voltage at the output of said first circuit enables the aging test to be performed by increasing [enlarging] the amplitude of the external supply voltage relative to an amplitude of normal operation voltage.

52. (amended) The semiconductor integrated circuit according to claim 23, further comprising:

a third circuit[,] supplied with the external supply voltage, [which] said third circuit transfers a signal to said internal circuit.

54. (amended) The semiconductor integrated circuit according to claim 52, wherein said third circuit has a larger device than a device [that] of said internal circuit.

57. (amended) The semiconductor integrated circuit according to claim 23, wherein said predetermined voltage is determined by a reference voltage [reference].

58. (amended) The semiconductor integrated circuit according to claim 57, wherein said reference voltage [reference] is determined by using a threshold voltage of said [first] MOS transistor.

59. (Amended) The semiconductor integrated circuit according to claim 23, wherein a [load] capacitance of a load of said [internal circuit] first circuit changes in accordance with a signal, said load includes said internal circuit.

60. (Amended) The semiconductor integrated circuit according to claim 27, wherein an [the] amplitude of [the

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output] a voltage at the output of said first circuit enables the aging test to be performed by increasing [enlarging] the amplitude of the external supply voltage relative to an amplitude of normal operation voltage.

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61. (amended) The semiconductor integrated circuit according to claim 49, wherein said second circuit [makes] causes a [the] changing rate of a voltage at the output [voltage] of said first circuit to be larger than the first rate during an aging test.

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62. (amended) The semiconductor integrated circuit according to claim 49, further comprising:

a third circuit[,] supplied with the external supply voltage, [which] said third circuit transfers a signal to said internal circuit.

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63. (amended) The semiconductor integrated circuit according to claim 58, further comprising:

a back bias generator supplying a back bias voltage to a region of the silicon substrate of the semiconductor integrated circuit.

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64. (amended) The semiconductor integrated circuit according to claim 58, wherein said third circuit has a larger device than a device [that] of said internal circuit.

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67. (amended) The semiconductor integrated circuit according to claim 27, wherein said predetermined voltage is determined by a reference voltage [reference].

68. (amended) The semiconductor integrated circuit according to claim 67, wherein said reference voltage [reference] is determined by using threshold voltage of a MOS transistor.

69. (amended) The semiconductor integrated circuit according to claim 27, wherein a [load] capacitance of a load of said [internal circuit] first circuit changes in accordance with a signal, said load includes said internal circuit.

70. (amended) A semiconductor integrated circuit comprising:

a first circuit[,] supplied with an external supply voltage, said first circuit [which] outputs [a] an output voltage whose amplitude has a first [small] dependence on an amplitude of the external supply voltage when the external supply voltage is larger than a predetermined voltage, wherein the amplitude of the output voltage of said first circuit is smaller than the amplitude of the external supply voltage;

a second circuit coupled to said first circuit for use in performing an aging test; and

an internal circuit supplied with the output voltage of said first circuit;

wherein said second circuit [makes] causes a second dependence, on the external supply voltage, of an [the] amplitude of a voltage at an [the] output [voltage] of said first circuit when the external supply voltage is larger than the predetermined voltage, to be larger than the first dependence.

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71. (amended) The semiconductor integrated circuit according to claim 70, wherein said first circuit includes a first MOS transistor having a source-drain path with which said internal circuit forms [makes] a current path, and

wherein an [the] output of said second circuit is coupled to the gate of said first MOS transistor.

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72. (amended) The semiconductor integrated circuit according to claim 70, wherein [the] an amplitude of an output voltage at the output [voltage] of said first circuit enables the aging test to be performed by increasing [enlarging] the amplitude of the external supply voltage relative to an amplitude of normal operation voltage.

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73. (amended) The semiconductor integrated circuit according to claim 70, wherein said second circuit [makes the] causes a dependence of an [the] amplitude of a voltage

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at the output [voltage] of said first circuit to be larger than the first dependence during the aging test.

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75. (amended) The semiconductor integrated circuit according to claim 70, further comprising:

a third [fourth] circuit[,] supplied with the external supply voltage, said third circuit [which] transfers a signal to said internal circuit.

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77. (amended) The semiconductor integrated circuit according to claim 75, wherein said third [fourth] circuit has a larger device than a device [that] of said internal circuit.

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78. (amended) The semiconductor integrated circuit according to claim 77, wherein said larger device of said third [fourth] circuit is a MOS transistor which has a larger thickness of the gate insulator than that of a MOS transistor of said internal circuit.

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79. (amended) The semiconductor integrated circuit according to claim 77, wherein said larger device of said third [fourth] circuit is a MOS transistor which has a longer gate length than that of a MOS transistor of said internal circuit.

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80. (amended) The semiconductor integrated circuit according to claim 70, wherein said predetermined voltage is determined by a reference voltage [reference].

81. (amended) The semiconductor integrated circuit according to claim 80, wherein said reference voltage [reference] is determined by using a threshold voltage of a MOS transistor.

82. (amended) The semiconductor integrated circuit according to claim 70, wherein said first circuit has a first MOS transistor having a source-drain path with which said internal circuit [makes] forms a current path, and a feedback circuit between the gate of said first MOS transistor and the output of said first circuit.

83. (amended) The semiconductor integrated circuit according to claim 70, wherein the [load] capacitance of a load of said [internal circuit] first circuit changes in accordance with a signal, said load includes said internal circuit.

84. (amended) The semiconductor integrated circuit according to claim 70, wherein an [the] output of said second circuit is coupled to the output of said first circuit.

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85. (amended) A semiconductor integrated circuit comprising:

a first circuit[,] supplied with an external supply voltage, said first circuit [which] outputs a voltage changing at a first rate which is smaller than the changing rate of the external supply voltage, when the external supply voltage changes to [in] a voltage [level] larger than a predetermined voltage;

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a second circuit coupled to said first circuit for use in performing an aging test; and

an internal circuit supplied with an output voltage of said first circuit;

wherein said second circuit [makes] causes a [the] changing rate of a voltage at an [the] output [voltage] of said first circuit to be larger than the first rate.

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86. (amended) The semiconductor integrated circuit according to claim 77, wherein said first circuit includes a first MOS transistor having a source-drain path with which said internal circuit [makes] forms a current path, and

wherein an [the] output of said second circuit is coupled to the gate of said first MOS transistor.

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87. (amended) The semiconductor integrated circuit according to claim 77, wherein an [the] amplitude of [the output] a voltage at the output of said first circuit enables the aging test to be performed by increasing

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[enlarging] the amplitude of the external supply voltage relative to an amplitude of normal operation voltage.

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88. (amended) The semiconductor integrated circuit according to claim 85, wherein said second circuit [makes] causes a [the] changing rate of a voltage at the output [voltage] of said first circuit to be larger than the first rate during the aging test.

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90. (amended) The semiconductor integrated circuit according to claim 85, further comprising:

a third [fourth] circuit[,] supplied with the external supply voltage, [which] said third circuit transfers a signal to said internal circuit.

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92. (amended) The semiconductor integrated circuit according to claim 90, wherein said third [fourth] circuit has a larger device than a device [that] of said internal circuit.

93. (amended) The semiconductor integrated circuit according to claim 92, wherein said larger device of said third [fourth] circuit is a MOS transistor which has a larger thickness of the gate insulator than that of a MOS transistor of said internal circuit.

94. (amended) The semiconductor integrated circuit according to claim 92, wherein said larger device of said third [fourth] circuit is a MOS transistor which has a longer gate length than that of a MOS transistor of said internal circuit.

95. (amended) The semiconductor integrated circuit according to claim 85, wherein said predetermined voltage is determined by a reference voltage [reference].

96. (amended) The semiconductor integrated circuit according to claim 95, wherein said reference voltage [reference] is determined by using a threshold voltage of a MOS transistor.

97. (amended) The semiconductor integrated circuit according to claim 85, wherein said first circuit has a first MOS transistor having a source-drain path with which said internal circuit forms [makes] a current path, and a feedback circuit between the gate of said first MOS transistor and the output of said first circuit.

98. (amended) The semiconductor integrated circuit according to claim 85, wherein a [the load] capacitance of a load of said [internal circuit] first circuit changes in accordance with a signal, said load includes said internal circuit.

99. (amended) The semiconductor integrated circuit according to claim 85, wherein an [the] output of said second circuit is coupled to the output of said first circuit.

100. (amended) A semiconductor integrated circuit comprising:

a first circuit[,] supplied with an external supply voltage, said first circuit [which] outputs a voltage changing at a first rate which is smaller than the changing rate of the external supply voltage, when the external supply voltage changes to [in] a [level] voltage larger than a predetermined voltage;

an internal circuit supplied with an [the] output [voltage] of said first circuit; and

a second circuit having a first MOS transistor whose source-drain path is coupled between the external supply voltage and the output of said first circuit;

wherein the first MOS transistor is turned on when said internal circuit requires, for an aging test, [needs] a larger voltage than the voltage changing at the first rate.

101. (amended) The semiconductor integrated circuit according to claim 100, wherein said first circuit includes a second MOS transistor having a source-drain path with which said internal circuit makes a current path, and

wherein an [the] output of said second circuit is coupled to the gate of said second MOS transistor.

102. (amended) The semiconductor integrated circuit according to claim 100, wherein the first MOS transistor is turned on during the aging test.

103. (amended) The semiconductor integrated circuit according to claim 100, further comprising:

a third circuit, supplied with the external supply voltage, [which] said third circuit transfers a signal to said internal circuit.

105. (amended) The semiconductor integrated circuit according to claim 103, wherein said third circuit has a larger device than a device [that] of said internal circuit.

108. (amended) The semiconductor integrated circuit according to claim 100, wherein said predetermined voltage is determined by a reference voltage [reference].

109. (amended) The semiconductor integrated circuit according to claim 108, wherein said reference voltage [reference] is determined by using a threshold voltage of a MOS transistor.

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110. (amended) The semiconductor integrated circuit according to claim 100, wherein said first circuit has a second MOS transistor having a source-drain path with which said internal circuit [makes] forms a current path, and a feedback circuit between the gate of said second MOS transistor and the output of said first circuit.

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111. (amended) The semiconductor integrated circuit according to claim 100, wherein [the load] a capacitance of a load of said [internal circuit] first circuit changes in accordance with a signal, said load includes said internal circuit.

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112. (amended) The semiconductor integrated circuit according to claim 100, wherein an [the] output of said second circuit is coupled to the output of said first circuit.

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113. (amended) A semiconductor integrated circuit comprising:

a first circuit[,] supplied with an external supply voltage, said first circuit [which] outputs a voltage changing at a first rate which is smaller than the changing rate of the external supply voltage, when the external supply voltage changes to [in] a [level] voltage larger than a predetermined voltage;

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an internal circuit supplied with an [the] output [voltage] of said first circuit; and

a second circuit having a first MOS transistor whose source-drain path is coupled between the external supply voltage and the output of said first circuit;

wherein the first MOS transistor is turned on for an aging test so that a voltage at the output of said first circuit is [can provide] a larger voltage than the voltage changing at the first rate.

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~~114~~. (amended) The semiconductor integrated circuit according to claim ~~113~~ 104, wherein said first circuit includes a second MOS transistor having a source-drain path with which said internal circuit forms [makes] a current path, and wherein the output of said second circuit is coupled to the gate of said second MOS transistor.

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~~115~~. (amended) The semiconductor integrated circuit according to claim ~~113~~ 104, wherein the first MOS transistor is turned on during the aging test.

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~~116~~. (amended) The semiconductor integrated circuit according to claim ~~113~~ 104, further comprising:

a third circuit, supplied with the external supply voltage, [which] said third circuit transfers a signal to said internal circuit.

118. (amended) The semiconductor integrated circuit according to claim 116, wherein said third circuit has a larger device than a device [that] of said internal circuit.

121. (amended) The semiconductor integrated circuit according to claim 113, wherein said predetermined voltage is determined by a reference voltage [reference].

122. (amended) The semiconductor integrated circuit according to claim 121, wherein said reference voltage [reference] is determined by using a threshold voltage of a MOS transistor.

123. (amended) The semiconductor integrated circuit according to claim 113, wherein said first circuit has a second MOS transistor having a source-drain path with which said internal circuit forms [makes] a current path, and a feedback circuit between the gate of said second MOS transistor and the output of said first circuit.

124. (amended) The semiconductor integrated circuit according to claim 113, wherein a [the load] capacitance of a load of said [internal circuit] first circuit changes in accordance with a signal, said load includes said internal circuit.

125. (amended) The semiconductor integrated circuit according to claim 113, wherein an [the] output of said second circuit is coupled to the output of said first circuit.

Please cancel claims 32, 74 and 89 without prejudice or disclaimer of the matter therein.

Please add new claims 126 and 127 as follows:

-- 126. A semiconductor integrated circuit comprising:

a first circuit supplied with an external supply voltage, said first circuit outputs an output voltage whose amplitude has a first dependence on an amplitude of the external supply voltage when the external supply voltage is larger than a predetermined voltage, wherein the amplitude of the output voltage of said first circuit is smaller than the amplitude of the external supply voltage;

a second circuit coupled to said first circuit for use in performing an aging test;

an internal circuit supplied with the output voltage of said first circuit;

wherein said second circuit causes a second dependence, on the external supply voltage, of an amplitude of a voltage at an output of said first circuit when the external supply voltage is larger than the predetermined voltage, to be larger than the first dependence; and

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a third circuit supplied with the external supply voltage, said third circuit transfers a signal to said internal circuit;

wherein said first circuit has a first MOS transistor having a source-drain path with which said internal circuit forms a current path, and a feedback circuit between the gate of said first MOS transistor and the output of said first circuit.

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127. A semiconductor integrated circuit comprising:

a first circuit supplied with an external supply voltage, said first circuit outputs a voltage changing at a first rate which is smaller than the changing rate of the external supply voltage, when the external supply voltage changes to a voltage larger than a predetermined voltage;

a second circuit coupled to said first circuit for use in performing an aging test;

an internal circuit supplied with an output voltage of said first circuit;

wherein said second circuit causes a changing rate of a voltage at an output of said first circuit to be larger than the first rate; and

a third circuit supplied with the external supply voltage, said third circuit transfers a signal to said internal circuit;

wherein said first circuit has a first MOS transistor having a source-drain path with which said